POWER GLITCH FREE INTERNAL VOLTAGE GENERATION CIRCUIT

Abstract of the Disclosure

A power glitch free internal voltage generation circuit includes: a voltage divider for dividing level of an internal voltage; a reference voltage generator generating a reference voltage having a predetermined voltage level by dividing a level of an external voltage; a comparator connected to the external voltage and the internal voltage and comparing the divided internal voltage with the reference voltage to generate a compared output; and a driver for supplying the external voltage to the internal voltage in response to the output of the comparator. In this manner, a high voltage level from either of the external voltage and the internal voltage is used as a source of the comparator. This, in turn, stably maintains the internal voltage because the driver for transferring the external voltage to the internal voltage is intercepted in the case where a glitch occurs that lowers the external voltage to a level lower than the internal voltage.